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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/466,961	12/20/1999	YOUN GYOUNG CHANG	8733.20050	1786
30827	7590 10/08/2003	·	EXAMINER	
MCKENNA LONG & ALDRIDGE LLP 1900 K STREET, NW			BROCK II, PAUL E	
	WASHINGTON, DC 20006			PAPER NUMBER
			2815	

DATE MAILED: 10/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
Office Action Commons	09/466,961	CHANG ET AL.				
Office Action Summary	Examiner	Art Unit				
	Paul E Brock II	2815				
Th MAILING DATE of this communication appears on the cov r sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status						
1) Responsive to communication(s) filed on <u>25</u> .	Responsive to communication(s) filed on <u>25 July 2003</u> .					
2a)⊠ This action is FINAL . 2b)□ Th	nis action is non-final.					
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213. Disposition of Claims						
4)⊠ Claim(s) <u>1,3,4,9,15,17,18 and 21</u> is/are pending in the application.						
	4a) Of the above claim(s) is/are withdrawn from consideration.					
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1,3,4,9,15,17,18 and 21</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/or election requirement. Application Papers						
9) The specification is objected to by the Examiner.						
10)☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
11)⊠ The proposed drawing correction filed on <u>31 August 2001</u> is: a)⊠ approved b)□ disapproved by the Examiner.						
If approved, corrected drawings are required in reply to this Office action.						
12) The oath or declaration is objected to by the Examiner.						
Priority under 35 U.S.C. §§ 119 and 120						
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).						
a)⊠ All b)□ Some * c)□ None of:						
1. Certified copies of the priority document	s have been received.					
2. Certified copies of the priority document	s have been received in Application	on No				
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 						
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).						
a) ☐ The translation of the foreign language provisional application has been received. 15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.						
Attachment(s)						
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s)	5) Notice of Informal F	y (PTO-413) Paper No(s) Patent Application (PTO-152)				

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DETAILED ACTION

Claim Rejections - 35 USC § 103

- 1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 2. Claims 1, 4 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bang in view of the applicant's admitted prior art.

With regard to claim 1, Bang discloses in figures 2b and 5g a switching TFT controlling a release of stored charges, the switching TFT having a gate electrode (11), an insulating layer (12) on the gate electrode, an active layer (13) on the insulating layer, an ohmic contact layer (15) on the active layer, and dual layered source and drain electrodes that are each comprised of a transparent conductive material (16 and 40) that extends over and contacts the ohmic contact layer, and a metal material (17 and 18) that extends over the transparent conductive material and that wraps around an end of the transparent conductive material to contact the ohmic contact layer. Bang is silent to a sensor TFT and a storage capacitor. The applicant's admitted prior art discloses in figure 1; page 2, lines 10 – 16; and page 3, lines 7 – 9 a sensor thin film transistor (TFT) (C) generating optical current. The applicant's admitted prior art further discloses in figure 1 a storage capacitor storing charges of the optical current generated in the sensor thin film transistor. It would have been obvious to one of ordinary skill in the art at the time of the present

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invention to use the sensor tft and the storage capacitor of the applicant's admitted prior art in the method of Bang in order to detect an optical image using well understood thin film transistors and capacitors as stated by the applicant's admitted prior art on page 2, lines 10 - 16.

With regard to claim 4, Bang discloses in column 6, lines 19 – 21 that the transparent conducting material is indium tin oxide.

With regard to claim 21, Bang discloses in figures 2b and 5g a switching TFT for selectively controlling a release of stored charges, the switching TFT having a gate electrode (11) on a first surface of a transparent substrate (100), an insulating layer (12) on the gate electrode, an active layer (13) on the insulating layer, an ohmic contact layer (15) on the active layer, and dual layered source and drain electrodes that are each comprised of a transparent conductive material (16 and 40) that extends over and contacts the ohmic contact layer, and a metal material (17 and 18) that extends over the transparent conductive material and that wraps around an end of the transparent conductive material to contact the ohmic contact layer. Bang discloses in figures 2b and 5g wherein the gate electrode blocks light passed by the first surface from reaching the active layer, and wherein the ohmic contact layer rests on the active layer. Bang is silent to a sensor TFT and a storage capacitor. The applicant's admitted prior art teaches in figure 1; page 2, lines 10 – 16; and page 3, lines 7 – 9 a sensor thin film transistor (TFT) (C) generating optical current. The applicant's admitted prior art further teaches in figure 1 a storage capacitor storing charges of the optical current. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the sensor TFT and the storage capacitor of the applicant's admitted prior art in the method of Bang in order to detect an optical image

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using well understood thin film transistors and capacitors as stated by the applicant's admitted prior art on page 2, lines 10 - 16.

3. Claims 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bang and the applicant's admitted prior art as applied to claims 1 above, and further in view of den Boer et al. (USPAT 5656824, den Boer).

Bang and the applicant's admitted prior art are silent to what material comprises the metal for the dual layered source and drain regions. den Boer teaches in figure 2; column 5, line 50; and column 7, lines 32 - 40 a substantially non-transparent metal layer (40) of chrome for a dual layer source electrode. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use non-transparent chrome layer of den Boer as the metal material in the dual layered electrodes of the applicant's admitted prior art and Bang in order to use a known metal whose processing is well understood in the art as taught by den Boer in column 7, lines 32 - 50.

4. Claims 15, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bang in view of the applicant's admitted prior art, and den Boer.

With regard to claim 15, Bang discloses in figures 2b and 5g a switching TFT. Bang discloses in figures 2b and 5g a gate electrode (11) on a transparent substrate (100). Bang discloses in figures 2b and 5g an insulating layer (12) over the gate electrode. Bang discloses in figures 2b and 5g a semiconductor layer on the insulating layer and adjacent the gate electrode, wherein the semiconductor layer includes an active layer (13) and an ohmic contact layer (15).

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Bang discloses in figures 2b and 5g spaced apart first (16 and 17) and second (40 and 18) switching electrodes on the semiconductor layer that define a channel region, wherein the second switching electrode electrically contacts the contact layer. Bang discloses in figures 2b and 5g wherein the second switching electrode is a dual layer structure comprised of a transparent conducting layer (40) that is in contact with the ohmic contact layer and a metal layer (18) that extends over the transparent conductive material and that wraps around an end of the transparent conductive material so as to contact the ohmic contact layer. Bang is silent to a sensor TFT and a storage capacitor. The applicant's admitted prior art discloses in figure 1; page 2, lines 10 – 16; and page 3, lines 7 – 9 a sensor thin film transistor (TFT) (C) having a gate electrode (11) and spaced apart first (27a) and second (27b) sensor electrodes. The applicant's admitted prior art further discloses in figure 1 a storage capacitor having a first storage electrode (13) and a second storage electrode (29), wherein the second storage electrode of the storage capacitor connects to the first sensor electrode and to a second switching electrode (31b). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the sensor TFT and the storage capacitor of the applicant's admitted prior art in the method of Bang in order to detect an optical image using well understood thin film transistors and capacitors as stated by the applicant's admitted prior art on page 2, lines 10 - 16. Bang and the applicant's admitted prior art are silent to what material comprises the metal for the dual layered electrode. den Boer teaches in figure 2; column 5, line 50; and column 7, lines 32 – 40 a non-transparent metal layer (40) of chrome for a dual layer electrode. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use non-transparent chrome layer of den Boer as the metal material in the dual layered electrode of the applicant's admitted prior

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art and Bang in order to use a known metal whose processing is well understood in the art as taught by den Boer in column 7, lines 32 – 50.

With regard to claim 17, Bang teaches in figures 2b and 5g wherein the transparent conducting layer contacts the side of the active layer.

5. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bang in view of den Boer.

With regard to claim 18, Bang discloses in figures 2b and 5 a gate electrode (11) on a substrate (100). Bang discloses in figures 2b and 5 an insulating layer (12) over the gate electrode. Bang discloses in figures 2b and 5 a semiconductor layer on the insulating layer and adjacent the gate electrode, wherein the semiconductor layer includes an active layer (13) and a contact layer (15). Bang discloses in figures 2b and 5 spaced apart first (16 and 17) and second (40 and 18) electrodes that electrically contact the contact layer so as to define a channel region. Bang discloses in figures 2b and 5 wherein the second electrode of the TFT is a dual layer structure comprised of a transparent conducting layer (40) that electrically contacts the contact—layer and a metal layer (18) that is disposed over the transparent conducting layer, wherein the metal layer extends over an end of the transparent conducting layer to electrically contact the contact layer. Bang is silent to what material comprises the metal for the dual layered source and drain regions. den Boer teaches in figure 2; column 5, line 50; and column 7, lines 32 – 40 a non-transparent metal layer (40) of chrome for a dual layer source electrode. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use non-transparent metal layer of den Boer as the metal material in the dual layered electrodes of Bang

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in order to use a known metal whose processing is well understood in the art as taught by den Boer in column 7, lines 32 - 50.

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Response to Arguments

- 6. Applicant's arguments filed July 25, 2003 have been fully considered but they are not persuasive.
- With regard to the applicant's argument that "this recitation of motivation fails to explain what specific scientific understanding or technological principle within the knowledge of one of ordinary skill in the art would have suggested the combination of the teachings of Bang and the Related Art," it should be noted that neither MPEP 2142 or In re Mills suggest that a "specific scientific understanding or technological principle" is required as proper motivation. It is submitted that proper motivation as required by law has been supplied. Therefore, applicant's arguments are not persuasive and the rejection is proper.
- 8. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5

 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

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In this case, the motivation has been given as "in order to detect an optical image using well understood thin film transistors and capacitors as stated by the applicant's admitted prior art on page 2, lines 10 - 16."

9. With regard to applicant's arguments citing In re GPAC, it should be noted that a full reading of GPAC is contrary to applicant's argument. In the cited section of GPAC the test for relevance is "In deciding whether a reference is from a relevant art, we first must determine whether the reference is within the inventor's filed of endeavor, and if it is not we next must determine whether the reference is reasonably pertinent to the particular problem confronting the inventor." In this case both the applicant's admitted prior art and Bang are related to semiconductor devices. In particular, both of the prior art references are related to thin film transistors. Applicant's field of endeavor is also thin film transistors. Therefore, according to GPAC, the references are in the applicant's field of endeavor, and a test of whether the prior art addresses the same problem need not be conducted. Further, according to In re Beattie, 24 USPQ2d 1040, 1042 (Fed. Cir. 1992) "As long as some motivation or suggestion to combine the references is provide by the prior art taken as a whole, the law does not require that the

references is provide by the prior art taken as a whole, the law does not require that the references be combined for the reasons contemplated by the inventor." Therefore, applicant's arguments are not persuasive, and the rejection is proper.

Conclusion

10. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II October 3, 2003

> EDDIE LEE SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2800